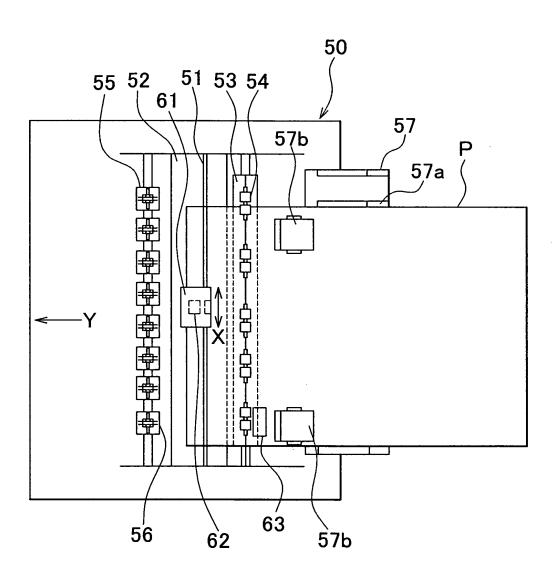
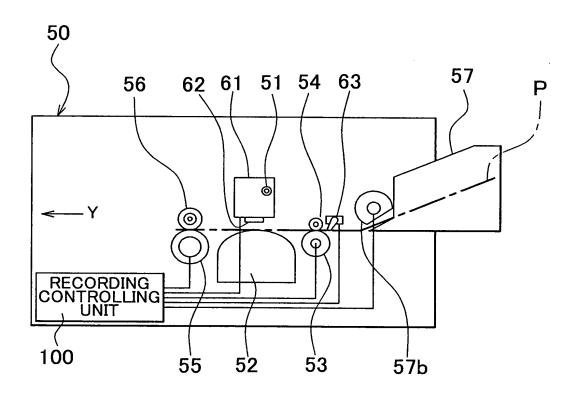


F I G. 1



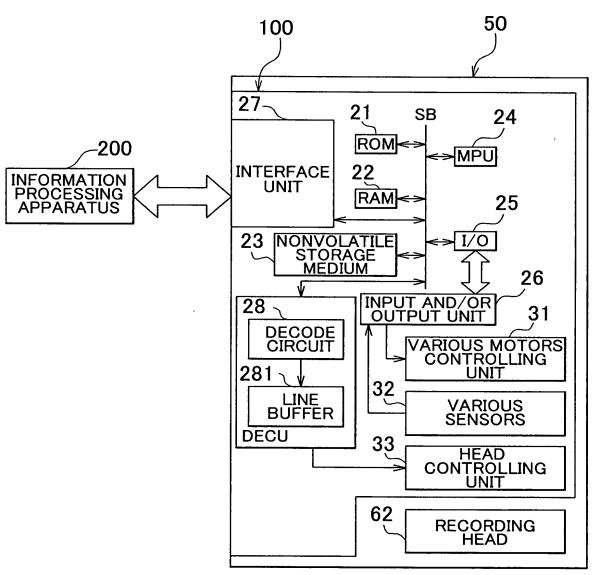


F I G. 2



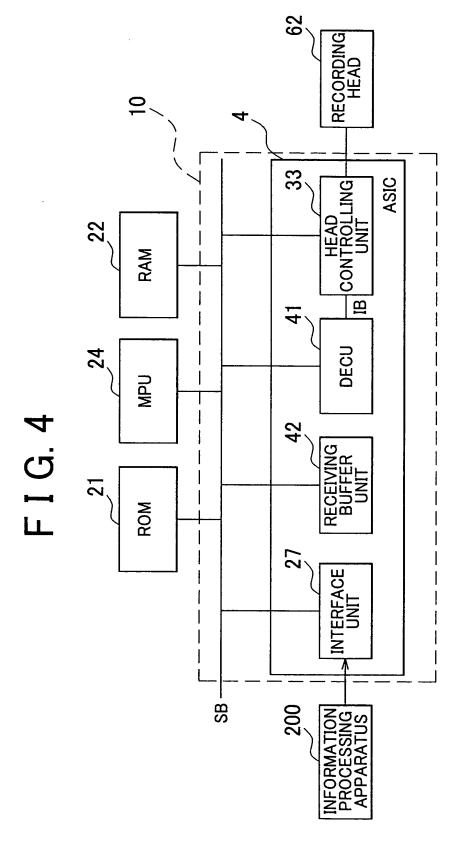


F I G. 3



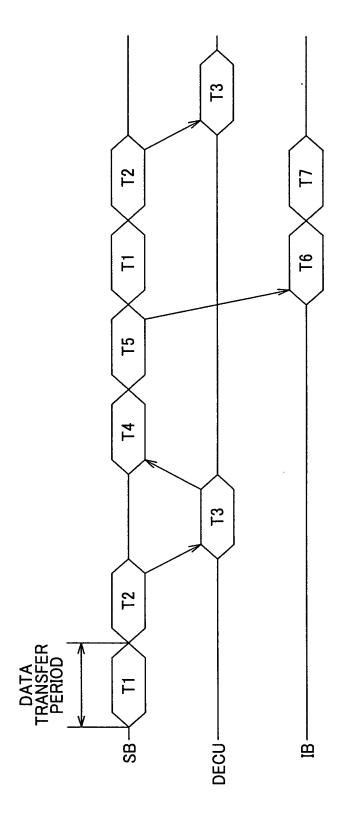
INKJET TYPE RECORDING APPARATUS







F I G. 5





I-DMA CONTROLLER MEMORY CONTROLLER 281 DECU DECODE CIRCUIT DEVELOPMENT PROCESSING CONTROLLER **LINE BUFFER** 402 SECOND S-DMA CONTROLLER FIRST S-DMA CONTROLLER F I G. 6 SB 425 RECEIVING BUFFER UNIT IF MEMORY

RAM

415

<u>@</u> ←

SB



F I G. 7

OPERATION CONDITION IF MEMORY SIDE: STARTING ADDRESS OF RUN LENGTH DATA IS AN EVEN ADDRESS SYSTEM MEMORY SIDE: STARTING ADDRESS OF IMAGE DATA IS AN EVEN ADDRESS NUMBER OF BYTES IN 1 LINE: 16 BYTES

DECU IF MEMORY TRANSFER SI FE 01 FACE A 01 01 01 FE 01 FACE B 03 02 TRANSFER S2 03 02 78 55 FACE A 01 01 01 02 44 FB FACE B FF FE TRANSFER S3 78 55 01 01 01 02 78 55 11 06 FACE A 66 12 FACE B 77 45 TRANSFER S4 44 FB 89 10 FACE A 01 01 01 02 78 55 44 55 FB FACE B 10 FA TRANSFER S5 FF FE 20 08 FACE A 01 01 01 02 78 55 44 FF FF FF FF FF 12 13 FACE B 14 15 TRANSFER S6 11 06 TRANSFER D1 FACE A 01 01 01 02 78 55 44 FF FF FF FF FF 11 11 11 16 17 18 19 FACE B 20 FD TRANSFER S7 66 12 11 02 FACE A 98 B0 FACE B 66 12 TRANSFER S8 77 45 F2 FC AB 03 FACE A FF FE FACE B 66 12 77 45 FC FD TRANSFER S9 89 10 FE FF FACE A FACE B 66 12 77 45 89 10 TRANSFER S10 55 FB FACE A FACE B 66 12 77 45 89 10 55 TRANSFER S11 10 FA FACE A FACE B 66 12 77 45 89 10 55 10 10 10 10 10 10 TRANSFER S12 20 08 TRANSFER D2 FACE A FACE B 66 12 77 45 89 10 55 10 10 10 10 10 10 20 20 20



F I G. 8

					:					
					•					
TRANSFER S13 12 13	1									
	20 20	20 20	12 13		1	F	ı	Γ		1
FACE B										
TRANSFER S14 14 15						1	L			ı
FACE A	20 20	20 20	12 13	14 15	1	Γ	1			1
FACE B		-								
TRANSFER S15 16 17										J
FACE A	20 20	20 20	12 13	14 15	16 17	l				1
FACE B										
TRANSFER S16 18 19										1
FACE A	20 20	20 20	12 13	14 15	16 17	18 19	1			
FACE B										
TRANSFER S17 20 FD										
FACE A	20 20	20 20	12 13	14 15	16 17	18 19	20			
FACE B							L			
TRANSFER S18 11 02									TR	ANSFER D3
FACE A	20 20	20 20	12 13	14 15	16 17	18 19	20 11	11 11		
FACE B	11									<u></u>
TRANSFER S19 98 BO										-
FACE A										
FACE B	11 98	B0 .					<u> </u>			
TRANSFER S20 F2 FC										•
FACE A					ļ					
FACE B	11 98	B0 F2		L	<u> </u>	L	<u> </u>	ا		ĺ
TRANSFER S21 AB 03										
FACE A	44.00						<u> </u>			
FACE B	11 98	B0 F2	AB AB	AR AR	IAB	L	<u> </u>	L		j
TRANSFER S22 FF FE						,				ı
FACE A	11.00	D0 E0	45.45	10.45			ļ			
FACE B	11 98	BU FZ	AR AR	AR AR	AB FF	FE	L	L		j
TRANSFER S23 FC FD						·	 			i
FACE A	11 98	B0 E2	AD AD	AD AD	AD E	FE EA	ED			
TRANSFER S24 FE FF	11 90	BU FZ	VD VB	VD VR	AB FF	ILE LO	ורט	L		 ANOCED 2.4
FACE A				Γ		1	·		18	ANSFER D4
	11 98	BU E3	AD AD	AD AD	AB EE	EE EA	FD FF	CC CC		\square
FACE B	11 30	שט רע		VD VD	AD LL	ILE LO	ILALL	ורד רד:		

DECU



SETTING CONDITION NO VERTICAL LINE REARRANGEMENT

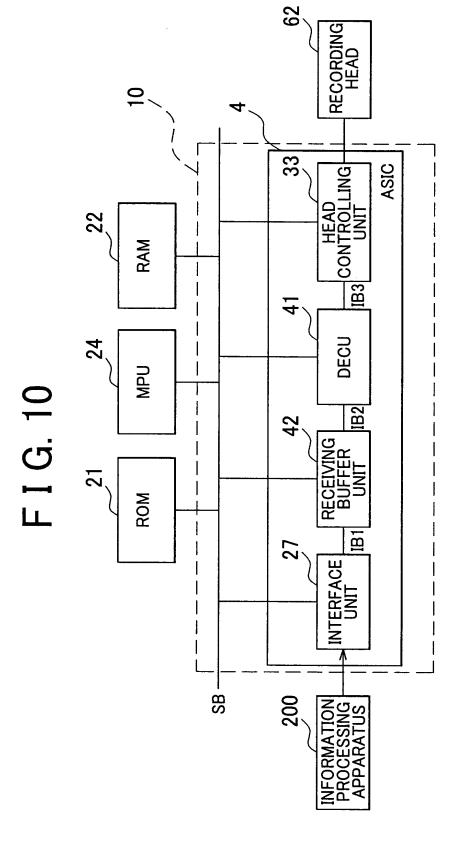
TOTAL NUMBER OF DEVELOPED BYTES: 64 BYTES(16 × 4)

NUMBER OF BYTES IN 1 LINE : 16BYTES NUMBER OF DEVELOPED LINES : 4 LINES

SYSTEM MEMORY

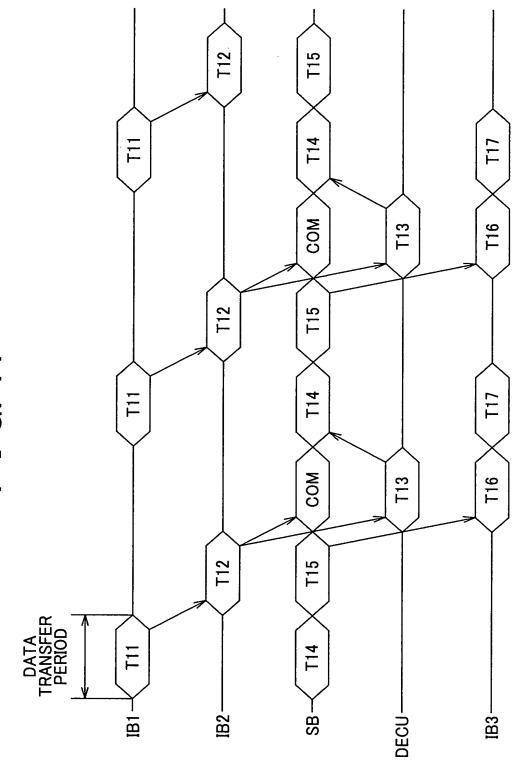
	SYSTEM MEMORY
FIG. 9A	D1— 01 01 01 02 78 55 44 FF FF FF FF FF FF 11 11 11 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
F I G. 9B	D2— 62 12 77 45 89 10 55 10 10 10 10 10 10 10 20 20 20 20 00 00 00 00 00 00 00 00 00
FIG. 9C	01 01 01 02 78 55 44 FF FF FF FF FF FF 11 11 11 62 12 77 45 89 10 55 10 10 10 10 10 10 20 20 20 20 20 20 20 12 13 14 15 16 17 18 19 20 11 11 11 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00
F I G. 9D	01 01 01 02 78 55 44 FF FF FF FF FF FF 11 11 11 62 12 77 45 89 10 55 10 10 10 10 10 10 20 20 20 20 20 20 20 12 13 14 15 16 17 18 19 20 11 11 11 D4— 11 98 B0 F2 AB AB AB AB AB FF FE FC FD FF FF





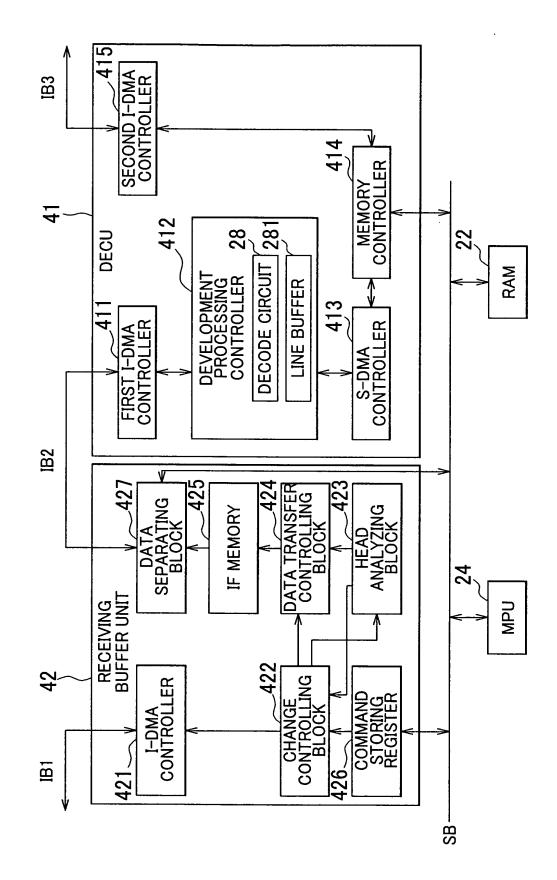


F I G. 11



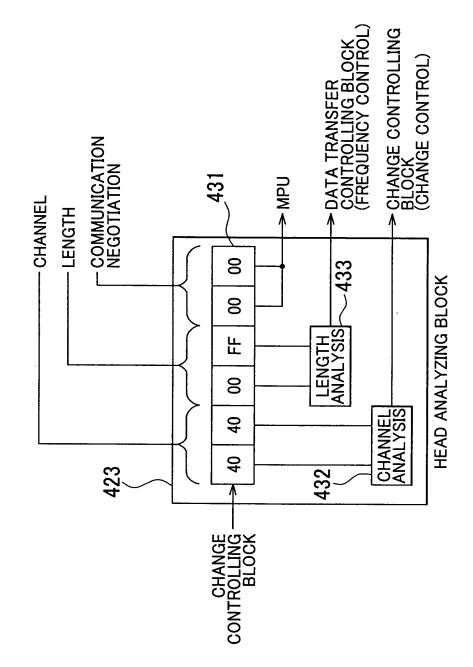


F I G. 12



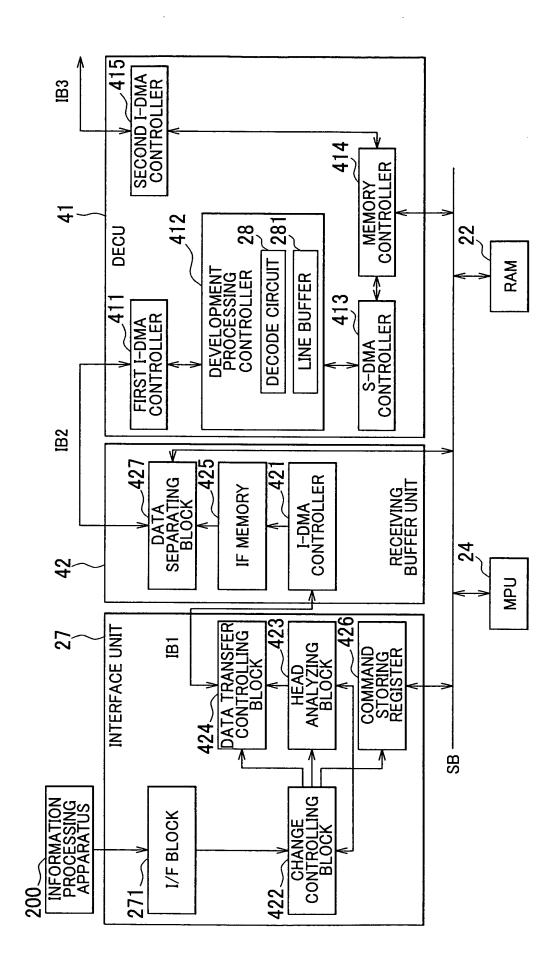


F I G. 13





F I G. 14





F I G. 15

